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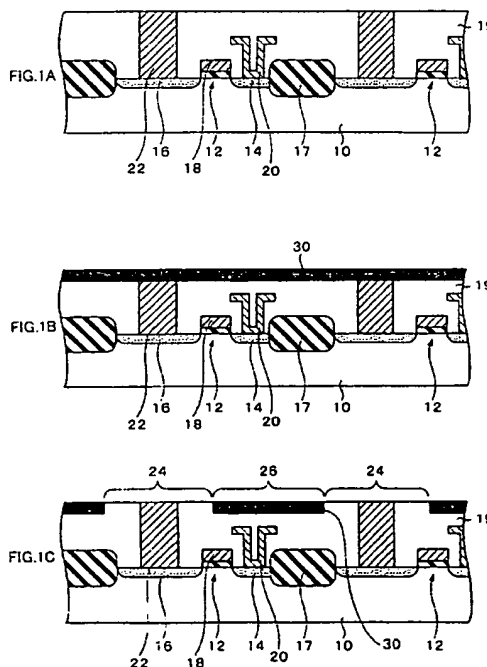
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(54) **FERROELECTRIC MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME**

(57) A method of manufacturing a ferroelectric memory device includes a step of forming a first region (24) having surface characteristics allowing the material for the members of a ferroelectric capacitor section to be preferentially deposited, and a second region (26) having surface characteristics allowing the material for the capacitor section to be less deposited than the first region (24), and a step of providing the material on the base (10) to form a first electrode (32), a ferroelectric film (34), and a second electrode (36) in the first region (24) of the base (10).



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Description

Technical Field

[0001] The present invention relates to a ferroelectric memory device and a method of manufacturing the same.

Background of Art

[0002] A ferroelectric memory (FeRAM) retains data by spontaneous polarization of a ferroelectric film used in capacitor sections. Conventionally, the capacitor sections are formed by dry etching using a reactive gas with a patterned photoresist as a mask.

[0003] Since the materials for forming the capacitor sections, in particular, platinum (Pt) and iridium (Ir) suitably used as the electrode materials exhibit low reactivity to etching gas, conventional technology has employed etching with an increased physical effect (sputter etching). In this case, by-products produced during etching are not removed in the vapor phase but are redeposited on the side wall of the resist pattern. It is very difficult to remove these redeposited by-products, which remain as a structure. As a method for preventing redeposition of by-products on the side wall of the resist pattern, a method of etching while moving the resist backward has been proposed. However, this etching method causes the side wall of the capacitor section to be sloped, whereby a high degree integration becomes difficult.

Disclosure of Invention

[0004] The present invention has been achieved to solve this problem. An object of the present invention is to provide a ferroelectric memory device which can be manufactured with high accuracy, and a method of manufacturing the same.

(1) The present invention provides a method of manufacturing a ferroelectric memory device provided with a capacitor section having a structure in which a first electrode, a ferroelectric film, and a second electrode are deposited, the method comprising the steps of:

forming a first region having surface characteristics allowing a material for forming at least one of the first electrode, the ferroelectric film, and the second electrode of the capacitor section to be preferentially deposited, and a second region having surface characteristics allowing a material for forming at least one member of the capacitor section to be less deposited than the first region; and providing the material for forming at least one member of the capacitor section to selectively

form the member in the first region.

According to the present invention, at least one member of the capacitor section can be selectively formed in the first region, but is less formed in the second region. Therefore, at least one of the first electrode, the ferroelectric film, and the second electrode can be formed without etching.

(2) In this method of manufacturing a ferroelectric memory device, the first region and the second region may be formed on the surface of a base.

According to this configuration, at least one member of the capacitor section can be selectively formed on the surface of the base. In particular, degradation of the ferroelectric film can be reduced by applying the present invention when forming the first electrode and the second electrode, thereby easily achieving miniaturization of devices.

(3) In this method of manufacturing a ferroelectric memory device,

the first electrode may be formed in the first region of the base by forming a layer of an electrode material on the base,
the ferroelectric film may be formed on the first electrode by forming a layer of a ferroelectric material on the base, and
the second electrode may be formed on the ferroelectric film by forming a layer of an electrode material on the base.

This enables the first electrode, the ferroelectric film, and the second electrode to be formed on the surface of the base in that order, whereby layers of all these members can be formed selectively.

(4) In this method of manufacturing a ferroelectric memory device,

the surface of the base may be exposed in the first region, and
a surface of the second region may be a surface-modifying film of which affinity to the electrode materials and the ferroelectric material is lower than an affinity of the exposed surface in the first region.

According to this configuration, affinity to the electrode materials and the ferroelectric material in the first region can be relatively increased by decreasing the affinity to the electrode materials and the ferroelectric material in the second region.

(5) This method of manufacturing a ferroelectric memory device may further comprise a step of removing the surface-modifying film after forming the first electrode, the ferroelectric film, and the second electrode.

(6) In this method of manufacturing a ferroelectric memory device,

the surface-modifying film may be formed on the base and selectively removed in a region which becomes the first region to form the surface-modifying film only in the second region.

(7) In this method of manufacturing a ferroelectric memory device, 5

the first electrode may be formed on the surface of the base, and a layer of the ferroelectric material is formed on the base and the first electrode, 10
the first region and the second region may be formed on the surface of the formed ferroelectric material, and
the second electrode may be formed in the first region by forming a layer of the electrode material on the formed ferroelectric material. 15

This enables the electrode material to be selectively formed on the surface of the formed ferroelectric material. 20

(8) This method of manufacturing a ferroelectric memory device may further comprise a step of removing the formed ferroelectric material in the region other than the second region after forming the second electrode. 25

(9) In this method of manufacturing a ferroelectric memory device,

the surface of the formed ferroelectric material may be exposed in the first region, and, 30
a surface of the second region may be a surface-modifying film of which affinity to the electrode material is lower than an affinity of the exposed surface of the formed ferroelectric material in the first region. 35

According to this configuration, affinity to the electrode material in the first region can be relatively increased by decreasing the affinity to the electrode material in the second region. 40

(10) In this method of manufacturing a ferroelectric memory device,

the surface-modifying may be formed on an entire surface of the base and the first electrode, 45
and selectively removed in a region which becomes the first region to form the surface-modifying film only in the second region.

(11) In this method of manufacturing a ferroelectric memory device, 50

the first electrode may be formed on a surface of the base, 55
the ferroelectric film may be formed on the first electrode,
the first region may be formed on an upper surface of the ferroelectric film,
the second region may be formed on surfaces

of the base and the ferroelectric film excluding the upper surface of the ferroelectric film, and the second electrode may be formed in the first region by forming a layer of an electrode material on the base on which the first electrode and the ferroelectric film are formed.

This enables the electrode material to be selectively formed on the upper surface of the ferroelectric film.

(12) In this method of manufacturing a ferroelectric memory device,

the step of forming the ferroelectric film may comprise:

a formation of a layer of an energy sensitive ferroelectric material on the base and the first electrode; and

a provision of energy to the formed ferroelectric material, thereby removing the ferroelectric material excluding a region which becomes the ferroelectric film.

This allows the ferroelectric film to be easily formed.

(13) In this method of manufacturing a ferroelectric memory device,

the upper surface of the ferroelectric film may be exposed in the first region, and
a surface of the second region may be a surface-modifying film of which affinity to the electrode material is lower than an affinity of the exposed surface of the ferroelectric film in the first region.

According to this configuration, affinity to a material for forming the electrode material in the first region can be relatively increased by decreasing the affinity to a material for forming the electrode material in the second region.

(14) This method of manufacturing a ferroelectric memory device may further comprise a step of removing the surface-modifying film after forming the second electrode.

(15) In this method of manufacturing a ferroelectric memory device, the surface-modifying film may be formed on an entire surface of the first electrode and the ferroelectric film, and selectively removed in a region which becomes the first region to form the surface-modifying film only in the second region.

(16) In this method of manufacturing a ferroelectric memory device,

a field effect transistor may be provided with a gate electrode, a source region, and a drain region which are formed on the base, and the ferroelectric memory device may have a

structure in which the first region corresponds to the electrode section connected to at least one of the source region and the drain region.

(17) In this method of manufacturing a ferroelectric memory device, a material for forming at least one member of the capacitor section may be selectively deposited in the first region by providing a material for forming the at least one member of the capacitor section using vapor phase growth.

Vapor phase growth is a process for supplying a material to be deposited in a vapor phase.

(18) In this method of manufacturing a ferroelectric memory device, the vapor phase growth may be chemical vapor deposition and a selective deposition process may be carried out in the first region.

(19) In this method of manufacturing a ferroelectric memory device, the second region may be formed above the first region.

(20) In this method of manufacturing a ferroelectric memory device which may comprise two or more the first regions,

a partition member may be formed between the first regions, and
the second region may be formed on the partition member.

According to this configuration, since the first regions are separated by the partition member, a problem in which the material for the ferroelectric film or the second electrode adheres to the side of the first electrode, or the material for the second electrode adheres to the side of the ferroelectric film can be prevented.

(21) In this method of manufacturing a ferroelectric memory device,

the partition member may be formed on the base, and
the second region may be formed at least on a surface of the partition member opposite to the base.

(22) In this method of manufacturing a ferroelectric memory device, the thickness of the partition member may be equal to or greater than the thickness of the capacitor section.

This prevents unnecessary material from adhering to the side of the capacitor section.

(23) This method of manufacturing a ferroelectric memory device may further comprise a step of removing the partition members.

(24) The present invention also provides a method of manufacturing a ferroelectric memory device provided with a capacitor section having a structure in which a base, a first electrode, a ferroelectric film, and a second electrode are deposited, the method

comprising the steps of:

forming, on a surface of the base, a first region having surface characteristics allowing a material for forming at least one of the first electrode, the ferroelectric film, and the second electrode of the capacitor section to be preferentially deposited, and a second region having surface characteristics allowing a material for forming at least one member of the capacitor section to be less deposited than the first region, and formed above the first region; and
providing a material for forming at least one member of the capacitor section to selectively form the member in the first region.

According to the present invention, the first region and the second region are formed on the surface of the base. At least one member of the capacitor section can be selectively formed in the first region, but is less formed in the second region. Therefore, at least one of the first electrode, the ferroelectric film, and the second electrode can be formed without etching. In particular, degradation of the ferroelectric film can be reduced by applying the present invention when forming the first electrode and the second electrode, thereby easily achieving miniaturization of the device.

(25) In this method of manufacturing a ferroelectric memory device,

the surface of the base may be exposed in the first region, and
a surface of the second region may be a surface-modifying film of which affinity to the materials for forming the members of the capacitor section is lower than an affinity of the exposed surface in the first region.

(26) This method of manufacturing a ferroelectric memory device may further comprise a step of removing the surface-modifying film after forming at least one of the first electrode, the ferroelectric film, and the second electrode.

(27) A ferroelectric memory device according to the present invention is manufactured using the above method.

(28) A ferroelectric memory device according to the present invention comprises:

a base having a first region and a second region;
a first electrode formed in the first region;
a ferroelectric film formed on the first electrode; and
a second electrode formed on the ferroelectric film,
wherein the second region has surface charac-

teristics allowing a material for forming at least one of the first electrode, the ferroelectric film, and the second electrode to be less deposited than a surface of the first region.

(29) In the ferroelectric memory device, the second region may be formed above a surface of the first region of the base.

(30) A ferroelectric memory device according to the present invention comprises:

a first electrode formed on a base;
a ferroelectric film formed on the first electrode;
and
a second electrode formed on the ferroelectric film,
wherein the base and the first electrode have surface characteristics allowing a material for forming the second electrode to be less deposited than a surface of the ferroelectric film on which the second electrode is formed.

(31) In this ferroelectric memory device, a transistor connected to at least one of the first electrode and the second electrode may be formed on the base.

Brief Description of Drawings

[0005] Figures 1A to 1C are views showing a method of manufacturing a ferroelectric memory device according to a first embodiment of the present invention.

[0006] Figures 2A to 2B are views showing the method of manufacturing a ferroelectric memory device according to the first embodiment of the present invention.

[0007] Figures 3A to 3B are views showing the method of manufacturing a ferroelectric memory device according to the first embodiment of the present invention.

[0008] Figure 4 is a plan view showing the ferroelectric memory device according to the first embodiment of the present invention.

[0009] Figure 5 is a view showing the circuit of the ferroelectric memory device according to the first embodiment of the present invention.

[0010] Figures 6A to 6C are views showing a method of manufacturing a ferroelectric memory device according to a second embodiment of the present invention.

[0011] Figures 7A to 7C are views showing the method of manufacturing a ferroelectric memory device according to the second embodiment of the present invention.

[0012] Figures 8A to 8C are views showing a method of manufacturing a ferroelectric memory device according to a third embodiment of the present invention.

[0013] Figures 9A to 9C are views showing the method of manufacturing a ferroelectric memory device according to the third embodiment of the present invention.

[0014] Figures 10A to 10C are views showing a method of manufacturing a ferroelectric memory device ac-

cording to a fourth embodiment of the present invention.

[0015] Figures 11A to 11C are views showing a method of manufacturing a ferroelectric memory device according to an embodiment of the present invention.

5 [0016] Figures 12A to 12B are views showing a method of manufacturing a ferroelectric memory device according to an embodiment of the present invention.

[0017] Figures 13 is a view showing an example of a modification of a method of manufacturing a ferroelectric memory device according to an embodiment of the present invention.

Best Mode for Carrying Out the Invention

15 [0018] Preferred embodiments of the present invention will be described below with reference to drawings.

First embodiment

20 [0019] Figures 1A to 3B are views showing a method of manufacturing a ferroelectric memory device according to a first embodiment of the present invention. A ferroelectric memory device is a nonvolatile semiconductor memory device. The minimum unit for storing information is a memory cell, which is formed by one transistor and one capacitor section, for example. A memory array can be formed by arraying a plurality of such memory cells. In this case, a plurality of memory cells can be arrayed in orderly rows and columns.

Formation of transistor

30 [0020] Transistors 12 which control the ferroelectric memory device are formed on a base 10 formed of a semiconductor wafer or the like, as shown in Figure 1A. A structure in which functional devices such as transistors are optionally formed on the base 10 corresponds to a base. The transistors 12 may have a conventional configuration, and may be thin film transistors (TFTs). In the case of MOSFETs, the transistors 12 include a drain/ source 14 and a drain/source 16 and a gate electrode 18. The gate electrode 18 is connected to a word line 44 (see Figure 4). An electrode 20, which is connected to the drain/source 14, is connected to a bit line 42 (see Figure 4). An electrode (plug) 22, which is connected to the drain/source 16, is connected to a first electrode 32 of the capacitor section of the ferroelectric memory device (see Figure 2A). Each memory cell is isolated by a LOCOS (Local Oxidation of Silicon) 17. An interlayer dielectric 19 formed of SiO₂ and the like is formed on the transistors 12.

Formation of capacitor section

55 [0021] The capacitor sections are formed as follows. First, a step of providing selectivity to the surface characteristics of the base in which the transistors 12 are formed on the base 10 is carried out. Selectivity is pro-

vided to the surface characteristics of the base by forming regions having different surface characteristics, such as wettability, for materials to be deposited on the surface of the base. In the present embodiment, first regions 24 (see Figure 1C) exhibiting affinity to the materials for forming the constituent members of the capacitor section, in particular, the materials for the electrodes, and a second region 26 (see Figure 1C) of which the affinity to the materials for forming the constituent members of the capacitor section is lower than that of the first regions 24 are formed on the interlayer dielectric 19 and the exposed area of the electrode (plug) 22 formed on the base 10. The capacitor sections of the ferroelectric memory device are selectively formed in the first regions 24 in a step described later, by utilizing the selectivity between each region, such as the deposition rate or adhesion to the base of the materials, caused by the difference in the surface characteristics. Specifically, at least one of the first electrodes 32, second electrodes 34, and ferroelectric films 34 of the capacitor sections is formed in the first regions 24 in a step described later, by a selective deposition process using chemical vapor deposition (CVD), physical vapor deposition, or a liquid phase process. In the case where the electrode (plug) 22 and the interlayer dielectric 19 formed on the base 10 have surface characteristics allowing the materials for forming the constituent members of the capacitor sections to be easily deposited, the surface of the base is exposed in the first regions 24 and a surface-modifying film 30 (see Figure 1C) on which these materials are less deposited extent is formed on the second region 26, thereby providing selectivity relating to the deposition of the materials for forming the constituent members of the capacitor sections.

Formation of surface-modifying film

[0022] In the present embodiment, the surface-modifying film 30 is formed over the entire surface of the base, as shown in Figure 1B. The surface-modifying film 30 is then removed in the first regions as shown in Figure 1C. The surface-modifying film 30 is allowed to remain in the second region 26. Specifically, the following steps are carried out.

[0023] The surface-modifying film 30 may be formed using vapor phase growth such as CVD or using a liquid phase process such as spin coating or dip coating. In the latter case, a liquid or a substance dissolved in a solvent is used. For example, a silane coupling agent (organosilicon compound) or a thiol compound can be used. A thiol compound is a generic name for organic compounds containing a mercapto group (-SH) (R^1 -SH; wherein R^1 represents a replaceable hydrocarbon group such as an alkyl group). Such a thiol compound is dissolved in an organic solvent such as dichloromethane or trichloromethane to prepare a solution with a concentration of about 0.1-10 mM, for example.

[0024] A silane coupling agent is a compound shown

by $R_n^2SiX_{4-n}$ (wherein n is a natural number, R^2 represents a hydrogen atom or a replaceable hydrocarbon group such as an alkyl group), in which X represents -OR³, -COOH, -OOCR³, -NH_{3-n}R³_n, -OCN, halogen, or the like (wherein R^3 represents a replaceable hydrocarbon group such as an alkyl group). Of these silane coupling agents and thiol compounds, compounds containing a fluorine atom in which R^1 or R^3 is $C_nF_{2n+1}C_mH_{2m}$ (wherein n and m are natural numbers) are particularly preferable. This is because these compounds increase surface free energy, thereby decreasing affinity to other materials.

[0025] Moreover, films produced using compounds containing a mercapto group or -COOH group using the above method may be used. Films formed from these materials may be used in the form of a monomolecular film or a built-up film thereof using an appropriate method.

Patterning of surface-modifying film

[0026] The surface-modifying film 30 is removed in the first regions 24, as shown in Figure 1C. In the case of forming the surface-modifying film 30 using a silane coupling agent, irradiation of light may cause the molecular bonds to be broken at the interface between the surface-modifying film 30 and the electrode (plug) 22 or interlayer dielectric 19 formed on the base 10, whereby the surface-modifying film 30 may be removed. Mask exposure used in lithography can be applied to such a patterning using light. Alternatively, the surface-modifying film 30 may be directly patterned using laser beams, electron beams, ion beams, or the like without using a mask.

[0027] The surface-modifying film 30 may be selectively formed in the second region 26 by transferring the surface-modifying film 30 formed on another base, thereby enabling layer formation and patterning of the surface-modifying film 30 at the same time.

[0028] The first regions 24 and the second region 26 covered with the surface-modifying film 30 are thus provided with different surface conditions, as shown in Figure 1C, thereby producing difference in the affinity to the materials for forming the constituent members of the capacitor sections formed in a step described later. In particular, in the case where the surface-modifying film 30 exhibits water repellency due to the presence of a fluorine molecule or the like, when using liquid materials for forming the constituent members of the capacitor sections, the materials can be selectively provided to the first regions 24. According to the material for the surface-modifying film 30, films may be formed in the first regions 24, on which the surface-modifying film 30 is not formed, using vapor phase growth due to the affinity to the materials for forming the upper layer members. As described above, each member of the capacitor sections of the ferroelectric memory device is formed in the succeeding steps by thus providing selectivity to the sur-

face characteristics of the first regions 24 and the second region 26.

Formation of first electrode

[0029] First electrodes 32 which become lower electrodes of the capacitor sections of the ferroelectric memory device are formed in the regions corresponding to the first regions 24, as shown in Figure 2A. Note that the term "in the regions corresponding to the first regions 24" means that the planar configuration of the first electrodes 32 may not be completely the same as the planar configuration of the plug 22. For example, a layer forming step using vapor phase growth is carried out for the entire surface of the base in which the transistors 12 are formed on the base 10. This causes a selective deposition process to occur. Specifically, a layer is formed in the first regions 24 but is less formed in the second region 26, whereby the first electrodes 32 are formed only in the first regions 24. As vapor phase growth, it is preferable to use CVD, in particular, MOCVD (Metal Organic Chemical Vapor Deposition). It is preferable that the material not be deposited in the second region 26. Note that it is sufficient that the layer forming rate in the second region 26 is at least two digits lower than in the first regions 24.

[0030] It is also preferable to form the first electrodes 32 using a method of selectively supplying a solution of the material to the first regions 24, or using mist deposition which selectively supplies mist of a solution of the material formed using ultrasonic means or the like to the first regions 24.

[0031] As the material for forming the first electrodes 32, Pt, Ir, or the like can be used. In the case of forming surface characteristic selectivity by forming the first regions 24 and the surface-modifying film 30 (second region 26) containing the above material on the base, the material for forming the electrodes can be selectively deposited using a compound containing Pt such as $(C_5H_7O_2)_2Pt$, $(C_5HFO_2)_2Pt$, or $(C_3H_5)(C_5H_5)Pt$, or a compound containing Ir such as $(C_3H_5)_3Ir$.

Formation of ferroelectric film

[0032] Ferroelectric films 34 are formed on the first electrodes 32, as shown in Figure 2B. Specifically, a layer forming step using vapor phase growth is carried out for the entire surface of the base, for example. Since the layer is formed on the first electrodes 32, but is less formed in the second region 26, the ferroelectric films 34 are formed only on the first electrodes 32. As vapor phase growth, CVD, in particular, MOCVD can be used.

[0033] It is also preferable to form the ferroelectric films 34 using a method of selectively supplying a solution of the material on the first electrodes 32 formed in regions other than the second region 26 using an ink jet method, or using mist deposition which selectively supplies mist of a solution of the material formed using ul-

trasonic means or the like to regions other than the second region 24.

[0034] The composition of the material for the ferroelectric films 34 may be appropriately determined insofar as the material exhibits ferroelectricity and can be used as a capacitor insulating film, and the layer can be formed using CVD. For example, PZT piezoelectric materials, materials to which niobium or a metal oxide such as nickel oxide or magnesium oxide is added, and the like can be used. Specific examples include lead titanate ($PbTiO_3$), lead zirconate titanate ($Pb(Zr,Ti)O_3$), lead zirconate ($PbZrO_3$), lanthanum titanate ($(Pb,La)TiO_3$), lanthanum lead zirconate titanate ($(Pb,La)(Zr,Ti)O_3$), lead magnesium niobate zirconium titanate ($Pb(Zr,Ti)(Mg,Nb)O_3$), and the like. In addition, SBT containing Sr, Bi, and Ta as constituent elements may be used.

[0035] In the case where surface characteristic selectivity is formed by forming the first region 24 and the surface-modifying film 30 (second region 26) which contains the above material on the base, the material for forming the ferroelectric films 34 can be selectively deposited using PZT containing a Pb compound such as $Pb(C_2H_5)_4$, $(C_2H_5)_3PbOCH_2C(CH_3)_3$, or $Pb(C_{11}H_{19}O_2)_2$, a Zr compound such as $Zr(n-OC_4H_9)_4$, $Zr(t-OC_4H_9)_4$, $Zr(C_{11}H_{19}O_2)_4$, or $Zr(C_{11}H_{19}O_2)_4$, and a Ti compound such as $Ti(i-C_3H_7)_4$, or STB containing an Sr compound such as $Sr(C_{11}H_{10}O_2)_2$, a Bi compound such as $Bi(C_6H_5)_3$, and a Ta compound such as $Ta(OC_2H_5)_5$.

Formation of second electrode

[0036] Second electrodes 36 which become upper electrodes are formed on the ferroelectric films 34, as shown in Figure 3A. Specifically, a layer forming step using vapor phase growth is preferably carried out for the entire surface of the base, for example. This causes the selective deposition process to occur. Specifically, since a layer is formed on the ferroelectric films 34, but is less formed in the second region 26, the second electrodes 36 are formed only on the ferroelectric films 34. As vapor phase growth, CVD, in particular, MOCVD can be applied.

[0037] It is also preferable to form the second electrodes 36 using a method of selectively supplying a solution of the material on the ferroelectric films 34 formed in regions other than the second region 26 using an ink jet method, or using mist deposition which forms mist of a solution of the material using ultrasonic means or the like and selectively supplies the mist to regions other than the second region 26.

[0038] The second electrodes 36 can be deposited by supplying an appropriate material prepared using a material similar to that for the first electrodes 32.

Removal of surface-modifying film, etc.

[0039] The surface-modifying film 30 formed in the second region 24 may be removed, as shown in Figure

3B. This step is carried out after completing the layer forming step using vapor phase growth. The surface-modifying film 30 may be removed using the above method of patterning the surface-modifying film 30, for example. It is preferable to remove substances adhering to the surface of the surface-modifying film 30 when removing the surface-modifying film 30. For example, the materials for the first electrodes 32, ferroelectric films 34, and second electrodes 36 adhering to the surface of the surface-modifying film 30 may be removed. Note that the step of removing the surface-modifying film 30 is not a necessary condition of the present invention. The surface-modifying film 30 may be allowed to remain.

[0040] In the case where the ferroelectric film 34 is formed on the side of the first electrode 32 or the second electrode 36 is formed on the side of at least either the first electrode 32 or the ferroelectric film 34, it is preferable to remove these materials. In the removal step, dry etching can be applied, for example.

[0041] In the present embodiment, the surface-modifying film 30 is formed in the second region 26, thereby providing the first regions 24 and the second region 26 with surface characteristics differing in the depositability of the material for forming at least one member (at least one of the electrodes and ferroelectric film) of the capacitor sections of the ferroelectric memory device. As a modification example, the surface-modifying film 30 may be formed in the first regions 24, and the material for forming at least one member of the capacitor section of the ferroelectric memory device may be provided with a liquid-phase or vapor-phase composition so as to be preferentially deposited on the surface of the surface-modifying film 30, thereby selectively forming the capacitor sections in the first regions 24.

[0042] Moreover, a thin layer of the surface-modifying film may be selectively formed on the surface of the second region 26, and at least one member of the capacitor sections of the ferroelectric memory device may be formed over the entire surface of the base including the first regions 24 and in the second region 26 by supplying a vapor-phase or liquid-phase material for that member. The material layer of this member may be selectively removed by polishing or a chemical technique only in the area where the thin layer of the surface-modifying film is formed, thereby selectively forming the material layer of this member in the first regions 24.

[0043] In addition, a film may not be formed on the surfaces of the first regions 24 and the second region 26. In this case, the surfaces of the first regions 24 and the second region 26 may be selectively provided with surface treatment so that the material for forming at least one member of the capacitor sections of the ferroelectric memory device is preferentially deposited in the first regions 24.

Structure of ferroelectric memory device

[0044] The ferroelectric memory device can be manufactured by these steps. According to the present embodiment, the first electrodes 32, the ferroelectric films 34, and the second electrodes 36 can be formed without etching using a mask.

[0045] This ferroelectric memory device includes the lower electrodes consisting of the first electrodes 32 formed on the first regions 24, the ferroelectric films 34 formed on the first electrodes 32, and the upper electrodes consisting of the second electrodes 36 formed on the ferroelectric films 34. The surface-modifying film 30 on which the vapor-phase or liquid-phase materials for forming the capacitor sections are less deposited in comparison with the surface of the base 10 may be formed in the second region 26 other than the first regions 24.

[0046] Figure 4 is a plan view showing a ferroelectric memory device according to an embodiment of the present invention. The ferroelectric memory device shown in Figure 4 has a 2T2C cell structure (2-transistor, 2-capacitor).

[0047] The transistors 12 are formed in regions 40. The electrodes 20 connected to the drain/source 14 (see Figure 3B) are connected to the bit lines 42 shown in Figure 4. The gate electrodes 18 (see Figure 3B) are connected to the word line 44 shown in Figure 4. The electrodes 22 connected to the drain/source 16 (see Figure 3B) are connected to a drive line 46 shown in Figure 4. The ferroelectric films 34 are formed on the electrodes 22 through the first electrodes 32.

[0048] Figure 5 is a view showing a circuit of the ferroelectric memory device according to the present embodiment. The action of the ferroelectric memory device will be described with reference to Figure 5.

[0049] In the case of writing data into the ferroelectric memory device, an address signal is supplied from an address terminal 51, a select signal is supplied from a chip-select terminal 52, and a write control signal is supplied from a write control terminal 53. A word line decoder/driver 50 turns ON the designated word line 44, with one of a plurality (two) of bit lines 42 turned ON, with the other bit line 42 turned OFF. A drive line decoder/driver 60 applies a positive pulse to the designated drive line 46. Then, residual polarization caused by the hysteresis characteristics of the ferroelectric film 34 remains in the ferroelectric capacitor, whereby information can be retained even if the power is turned off.

[0050] In the case of reading data from the ferroelectric memory device, the bit line 42 is left floating and the word line 44 is turned ON, thereby selecting the memory cell. Then, a positive voltage is applied to the drive line 46 and displacement current caused by polarization inversion of the ferroelectric capacitor is amplified using a sense amplifier 70. A sense timing control section 80 controls sense timing and supplies data to a data I/O 90. The data I/O 90, which is connected to a device 92 in-

cluding a CPU and other memory devices, controls data transmission.

[0051] The present invention is not limited to the above embodiment and various modifications are possible. For example, instead of forming all of the first electrodes 32, ferroelectric films 34, and second electrodes 36 by the selective deposition process, at least one of these members may be formed by the selective deposition process. In particular, it is unnecessary to perform etching by applying the selective deposition process when forming the first electrode 32 and the second electrode 36, thereby preventing degradation of the characteristics of the ferroelectric films 34.

Second embodiment

[0052] Figures 6A to 7C are views showing a method of manufacturing a ferroelectric memory device according to a second embodiment of the present invention. In the present embodiment, capacitor sections are formed on a base 110 shown in Figure 6A. The description for the base 10 in the first embodiment is applicable to the base 110.

Formation of first electrode

[0053] First electrodes (lower electrodes) 132 are formed on the base 110, as shown in Figure 6A. The first electrodes 132 are formed by forming a layer of an electrode material for the first electrodes 132 on the base 110 and patterning the formed electrode material, for example.

[0054] There are no specific limitations to the electrode material insofar as the material has a function of forming part of the ferroelectric capacitor. For example, in the case of using lead zirconate titanate (PZT) as the material for forming ferroelectric films 134 (see Figure 7C), a monolayer or lamination layer of platinum (Pt), iridium (Ir), compounds thereof, and the like is suitable as the electrode material for the first electrodes 132.

[0055] As the method of forming a layer of the electrode material, sputtering, vacuum evaporation, CVD, or the like can be used. As the patterning method, lithographic technology can be used. In addition, the selective deposition process described in the first embodiment may be used.

Layer forming of ferroelectric material

[0056] A layer of a ferroelectric material 133 is formed as shown in Figure 6B. Specifically, the ferroelectric material 133 is formed on the surface (may be the entire surface) of the base 110 on which the first electrodes 132 are formed so as to cover the first electrodes 132.

[0057] As the composition of the ferroelectric material 133, perovskite oxide ferroelectrics such as lead titanate, lead zirconate titanate (PZT), and lead zirconate; bismuth-based layered oxides such as strontium bis-

muth tantalate (SBT); organic polymer ferroelectrics such as polyvinylidene fluoride, vinylidene fluoride/ethylene trifluoride copolymer, and vinylidene cyanide/vinyl acetate copolymer; or the like can be used.

[0058] As the method of forming a layer of the ferroelectric material 133, sputtering, CVD (MOCVD), sol-gel process, MOD, or the like can be used. For example, in the case of forming a layer of the ferroelectric material 133 using lead zirconate titanate by a sol-gel process, a solution (sol) in which titanium tetraisopropoxide, tetra-n-propoxyzirconium, and lead acetate are dissolved in an organic solvent such as 2-n-butoxyethanol and diethanolamine is used.

15 Formation of surface-modifying film

[0059] A surface-modifying film 130 is formed on the surface (may be the entire surface) of the formed ferroelectric material 133, as shown in Figure 6C. The description for the surface-modifying film 30 in the first embodiment is applicable to the surface-modifying film 130, which is formed in the same manner as the surface-modifying film 30.

25 Patterning of surface-modifying film

[0060] The surface-modifying film 130 formed on the formed ferroelectric material 133 is removed in the regions where the first electrodes 132 are formed, as shown in Figure 7A. The surface-modifying film 130 is allowed to remain in a second region 126. As a method of patterning the surface-modifying film 130, the patterning method for the surface-modifying film 30 described in the first embodiment can be applied.

[0061] As a result of these steps, the surface conditions of the formed ferroelectric material 133 differ between first regions 124 and the second region 126 which is covered with the surface-modifying film 130, as shown in Figure 7A. This produces a difference in the affinity to the electrode material for forming second electrodes 136.

[0062] In the present embodiment, the surface-modifying film 130 is removed in the regions corresponding to the first electrodes 132. The above description should not be construed as limiting the present invention. The surface-modifying film 130 may be selectively removed according to the structure (formation region) of the second electrodes necessary for the structure of the device to be manufactured.

Formation of second electrode

[0063] The second electrodes 136 are formed by selectively depositing the electrode material in the regions corresponding to the first regions 124, as shown in Figure 7B. As the deposition method, sputtering, CVD (MOCVD), sol-gel process, MOD, electroplating, electroless plating, or the like can be used. The details are

the same as described for the first electrode 32 in the first embodiment.

Etching of formed ferroelectric material

[0064] The formed ferroelectric material 133 is etched, as shown in Figure 7C. Specifically, the ferroelectric material 133 is etched using the second electrodes 136 as masks.

[0065] As the etching method, parallel-plate reactive ion etching (RIE), dry etching using a plasma source such as inductively coupled plasma (ICP) or electron cyclotron resonance (ECR), or the like can be used.

[0066] There are no specific limitations to the etching gas insofar as the formed ferroelectric material 133 can be etched. For example, in the case of using PZT as the ferroelectric material 133, fluorine-based gas such as CF_4 , C_4F_8 , and C_5F_8 , chlorine-based gas such as Cl_2 and BCl_3 , Ar, O_2 , and the like can be used individually or in combination of two or more. It is particularly preferable to use fluorine-based gas. Use of fluorine-based gas increases etching selectivity of the ferroelectric material 133 for Pt or Ir which is suitably used as the constituent material for the first electrodes 132 and the second electrodes 136.

[0067] The ferroelectric memory device can be manufactured by these steps, as shown in Figure 7C. According to the present embodiment, the second electrodes 136 can be formed without etching.

Third embodiment

[0068] Figures 8A to 9C are views showing a method of manufacturing a ferroelectric memory device according to a third embodiment of the present invention. In the present embodiment, capacitor sections are formed on the base 110 shown in Figure 8A. The description for the base 10 in the first embodiment is applicable to the base 110.

Formation of first electrode

[0069] The first electrodes 132 (lower electrodes) are formed on the base 110, as shown in Figure 8A. The details are described in the second embodiment.

Layer formation of ferroelectric material

[0070] A layer of a ferroelectric material 233 is formed, as shown in Figure 8A. Specifically, a layer of the ferroelectric material 133 is formed on the surface of the base 110 on which the first electrodes 132 are formed to cover the first electrodes 132.

[0071] As the composition of the ferroelectric material 233, perovskite oxide ferroelectrics such as lead titanate, lead zirconate titanate (PZT), and lead zirconate; bismuth-based layered oxides such as strontium bismuth tantalate (SBT); organic polymer ferroelectrics

such as polyvinylidene fluoride, vinylidene fluoride/ethylene trifluoride copolymer, and vinylidene cyanide/vinyl acetate copolymer; or the like can be used.

[0072] In the present embodiment, a ferroelectric material exhibiting patterning characteristics upon irradiation with energy rays is used as the ferroelectric material (precursor) 233. The term "patterning characteristics upon irradiation with energy rays" means that the crosslinking reaction, decomposition reaction, modification reaction, or the like of the ferroelectric material (precursor) 233 is induced by energy rays, whereby either the irradiated region or unirradiated region can be selectively removed using a chemical solution.

[0073] For example, a raw material solution, in which orthonitrobenzaldehyde (photosensitizer) is added to a solgel solution containing lead acetate (II) trihydrate, zirconium tetra-n-butoxide, and titanium tetraisopropoxide which is distilled using 2-methoxyethanol, is applied to the base 110 using spin coating. The applied solution is dried on a hot plate at 95°C for 1 hour to form a precursor film with a predetermined thickness.

[0074] As the application method, roll coating, spray coating, dip coating, or the like can be used other than spin coating.

[0075] The formed ferroelectric material 233 is then patterned. For example, the ferroelectric material 233 is removed in the regions in which the first electrode 132 is not formed, as shown in Figure 8C. The ferroelectric material 233 is allowed to remain on the first electrodes 132.

[0076] For example, the formed ferroelectric material 233 is exposed to light with a wavelength of 365 nm through a reticle (mask, not shown), as shown in Figure 8B. The reticle (mask) has a shading layer formed so as to transmit light only in the region corresponding to the region in which the ferroelectric films 234 will be formed (see Figure 8C).

[0077] In the present embodiment, light with a wavelength of 365 nm is used corresponding to orthonitrobenzaldehyde used as the photosensitizer. Light (energy ray) with various wavelengths can be used by changing the photosensitizer.

[0078] Then, the unexposed area is removed by developing the ferroelectric material 233 for 60-120 minutes using a developer in which 2-methoxyethanol and isopropyl alcohol are mixed in a ratio of 1:1, thereby patterning the precursor film. The precursor film is heated on a hot plate at 350°C for 10 minutes. The above steps are repeated until the desired film thickness is obtained.

[0079] The resulting precursor film is crystallized by annealing at 600°C for 60 minutes in an annealing furnace, thereby obtaining the patterned ferroelectric films 234, as shown in Figure 8C.

Formation of surface-modifying film

[0080] A surface-modifying film 230 is formed on the surface (may be the entire surface) of the base 110 on

which the first electrodes 132 and the ferroelectric films 234 are formed, as shown in Figure 9A. The surface-modifying film 230 is formed to cover the exposed surface of the base 110 from the first electrodes 132 and the ferroelectric films 234, the upper surface and the side of the ferroelectric films 234, and the side of the first electrodes 132. The description for the surface-modifying film 30 in the first embodiment is applicable to the surface-modifying film 230.

Patterning of surface-modifying film

[0081] The upper surface of the ferroelectric films 234 is exposed by removing the surface-modifying film 230 from at least part of the surface of the ferroelectric films 234, thereby forming first regions 224. The surface-modifying film 230 is allowed to remain in another region which becomes a second region 226. As a result, the material for forming second electrodes 236 is less deposited in the second region 226 (the surface of the base 110, the side of the first electrodes 132, and the side of the ferroelectric film 234) by the presence of the surface-modifying film 230, in comparison with the first regions 224.

[0082] As the method of patterning the surface-modifying film 230, the method of patterning the surface-modifying film 30 in the first embodiment can be applied.

[0083] As a result of these steps, the surface conditions differ between the first regions 224 and the second region 226 which is covered with the surface-modifying film 130, as shown in Figure 9B, thereby producing a difference in the affinity to the electrode material for forming the second electrodes 236.

Formation of second electrode

[0084] The second electrodes 236 are formed by selectively depositing the electrode material in the regions corresponding to the first regions 224, as shown in Figure 9C. As the deposition method, sputtering, CVD (MOCVD), sol-gel process, MOD, electroplating, electroless plating, or the like can be used. Other details are as described for the first electrodes 32 in the first embodiment. Specifically, in the present embodiment, the second electrodes 236 are formed in the same manner as the first electrodes 32 in the first embodiment.

Removal of surface-modifying film, etc.

[0085] The surface-modifying film 130 shown in Figure 9C may be removed, as required. The details are described in the first embodiment. Note that the step of removing the surface-modifying film 230 is not a necessary condition of the present invention. The surface-modifying film 230 may be allowed to remain.

[0086] The ferroelectric memory device can be manufactured by these steps. According to the present embodiment, the second electrodes 236 can be formed

without etching. Moreover, in the present embodiment, the ferroelectric film 234 is also formed without etching.

Fourth embodiment

[0087] Figures 10A to 12B are views showing a method of manufacturing a ferroelectric memory device according to a fourth embodiment of the present invention.

10 Formation of transistor and capacitor section

[0088] The transistors 12 and the capacitor sections are formed on the base 10, as shown in Figure 10A. The details are described in the first embodiment. A second region 326 is formed above the first regions 24 with respect to the base 10. The capacitor sections of the ferroelectric memory device are formed in the first regions 24 in a step described later.

20 Formation of partition member

[0089] In the present embodiment, partition members 328 are formed as shown in Figure 10B. The partition members 328 are formed in regions other than the regions in which the capacitor sections of the ferroelectric memory device are formed (first regions 24). It is preferable that the partition members 328 separate the regions for forming the capacitor sections. The thickness of the partition members 328 is preferably equal to or greater than that of the capacitor sections.

[0090] As the partition members 328, an insulating material such as SiO₂, SiN, or TiO₂ can be used. If the material is removed in the succeeding step, Au or the like may be used. The partition members 328 are formed by forming a layer of the material over the entire surface of the base and patterning the film so as to be present in regions other than the first regions 24 using photolithography and etching.

40 Formation of surface-modifying film

[0091] In the present embodiment, a surface-modifying film 330 is formed as shown in Figure 10c. The region in which the surface-modifying film 330 is formed becomes the second region 326. For example, the surface-modifying film 330 is formed over the entire surface of the base on which the partitions are formed, and the surface-modifying film 330 is then removed in the region other than at least the upper surface of the partition members 328. The details are as described in the first embodiment.

Patterning of surface-modifying film

[0092] After forming the surface-modifying film 330 over the entire surface of the base, the surface-modifying film 330 is removed in the first regions 24. The surface-modifying film 330 on the side of the partition mem-

bers 328 may be removed. The details are as described in the first embodiment.

Formation of first electrode

[0093] The first electrodes 32 which become the lower electrodes of the capacitor sections of the ferroelectric memory device are formed in the regions corresponding to the first regions 24, as shown in Figure 11A. The details are as described in the first embodiment.

Formation of ferroelectric film

[0094] The ferroelectric films 34 are formed on the first electrodes 32, as shown in Figure 11B. The details are described in the first embodiment.

[0095] In the present embodiment, since the first regions 24 are separated by the partition members 328, the side of the first electrodes 32 are in contact with the partition members 328. Therefore, the material for the ferroelectric films 34 does not adhere to the side of the first electrodes 32.

Formation of second electrode

[0096] The second electrodes 36 which become the upper electrodes are formed on the ferroelectric films 34, as shown in Figure 11C. The details are as described in the first embodiment.

[0097] In the present embodiment, since the first regions 24 are separated by the partition members 328, the sides of the first electrodes 32 and the ferroelectric films 34 are in contact with the partition members 328. Therefore, the material for the second electrodes 36 does not adhere to the side of the first electrode 32 and the ferroelectric film 34.

Removal of surface-modifying film, etc.

[0098] The surface-modifying films 330 constituting the second region 326 may be removed, as shown in Figure 12A. The details are as described in the first embodiment.

[0099] Moreover, the partition members 328 may be removed, as shown in Figure 12B. This step is not a necessary condition of the present invention, and the partition members 328 may be allowed to remain. In the present embodiment, the surface of the second region 326 is formed by the upper surface of the partition member 328.

Structure of ferroelectric memory device

[0100] The ferroelectric memory device can be manufactured by these steps. According to the present embodiment, the first electrodes 32, the ferroelectric films 34, and the second electrodes 36 can be formed without etching using a mask. Since the first regions 24 are sep-

arated by the partition members 328, at least one of the materials for the ferroelectric films 34 and the second electrodes 36 can be prevented from adhering to the sides of first electrodes 32. Moreover, the material for the second electrodes 36 can be prevented from adhering to the sides of the ferroelectric films 34. In particular, since the material for the second electrodes 36 can be prevented from adhering to the sides of the ferroelectric films 34, a problem in which the capacitor section cannot be formed due to conduction between the first electrodes 32 and the second electrodes 36 can be prevented.

[0101] In this ferroelectric memory device, the partition members 328 may be formed in the region other than the first regions 24. The second region 326, in which the vapor-phase or liquid-phase material for the capacitor section is less deposited in comparison with the surface of the base, may be formed using the surface-modifying film 330 or the like. The second region 326 may be formed on the upper surface of the partition members 328.

[0102] The present invention is not limited to the above-described embodiment and various modifications are possible. For example, instead of forming all of the first electrode 32, ferroelectric film 34, and second electrode 36 by the selective deposition process, at least one of these may be formed by the selective deposition process. In particular, it is unnecessary to perform etching by applying the selective deposition process when forming the first electrode 32 and the second electrode 36, thereby preventing degradation of the characteristics of the ferroelectric film 34.

[0103] In the present embodiment, the surface-modifying film 330 is formed on the upper surface of the partition members 328. The surface-modifying film 330 may be formed on the upper surface and the sides of the partition members 328. In this case, the upper surface and the sides of the partition members 328 form a second region 327 having surface characteristics in which the material for forming at least one member of the capacitor section is less deposited.

Claims

1. A method of manufacturing a ferroelectric memory device provided with a capacitor section having a structure in which a first electrode, a ferroelectric film, and a second electrode are deposited, the method comprising the steps of:

forming a first region having surface characteristics allowing a material for forming at least one of the first electrode, the ferroelectric film, and the second electrode of the capacitor section to be preferentially deposited, and a second region having surface characteristics allowing a material for forming at least one mem-

- ber of the capacitor section to be less deposited than the first region; and providing the material for forming at least one member of the capacitor section to selectively form the member in the first region.
2. The method of manufacturing a ferroelectric memory device as defined in claim 1, wherein the first region and the second region are formed on the surface of a base.
 3. The method of manufacturing a ferroelectric memory device as defined in claim 2, wherein the first electrode is formed in the first region of the base by forming a layer of an electrode material on the base, wherein the ferroelectric film is formed on the first electrode by forming a layer of a ferroelectric material on the base, and wherein the second electrode is formed on the ferroelectric film by forming a layer of an electrode material on the base.
 4. The method of manufacturing a ferroelectric memory device as defined in claim 3, wherein the surface of the base is exposed in the first region, and wherein a surface of the second region is a surface-modifying film of which affinity to the electrode materials and the ferroelectric material is lower than an affinity of the exposed surface in the first region.
 5. The method of manufacturing a ferroelectric memory device as defined in claim 4, further comprising a step of removing the surface-modifying film after forming the first electrode, the ferroelectric film, and the second electrode.
 6. The method of manufacturing a ferroelectric memory device as defined in claim 4, wherein the surface-modifying film is formed on the base and selectively removed in a region which becomes the first region to form the surface-modifying film only in the second region.
 7. The method of manufacturing a ferroelectric memory device as defined in claim 1, wherein the first electrode is formed on the surface of the base, and a layer of the ferroelectric material is formed on the base and the first electrode, wherein the first region and the second region are formed on the surface of the formed ferroelectric material, and wherein the second electrode is formed in the first region by forming a layer of the electrode material on the formed ferroelectric material.
 8. The method of manufacturing a ferroelectric memory device as defined in claim 7, further comprising a step of removing the formed ferroelectric material in the region other than the second region after forming the second electrode.
 9. The method of manufacturing a ferroelectric memory device as defined in claim 8, wherein the surface of the formed ferroelectric material is exposed in the first region, and, wherein a surface of the second region is a surface-modifying film of which affinity to the electrode material is lower than an affinity of the exposed surface of the formed ferroelectric material in the first region.
 10. The method of manufacturing a ferroelectric memory device as defined in claim 9, wherein the surface-modifying film is formed on an entire surface of the base and the first electrode, and selectively removed in a region which becomes the first region to form the surface-modifying film only in the second region.
 11. The method of manufacturing a ferroelectric memory device as defined in claim 1, wherein the first electrode is formed on a surface of the base, wherein the ferroelectric film is formed on the first electrode, wherein the first region is formed on an upper surface of the ferroelectric film, wherein the second region is formed on surfaces of the base and the ferroelectric film excluding the upper surface of the ferroelectric film, and wherein the second electrode is formed in the first region by forming a layer of an electrode material on the base on which the first electrode and the ferroelectric film are formed.
 12. The method of manufacturing a ferroelectric memory device as defined in claim 11, wherein the step of forming the ferroelectric film comprises: a formation of a layer of an energy sensitive ferroelectric material on the base and the first electrode; and a provision of energy to the formed ferroelectric material, thereby removing the ferroelectric material excluding a region which becomes the

ferroelectric film.

13. The method of manufacturing a ferroelectric memory device as defined in claim 11,

wherein the upper surface of the ferroelectric film is exposed in the first region, and wherein a surface of the second region is a surface-modifying film of which affinity to the electrode material is lower than an affinity of the exposed surface of the ferroelectric film in the first region.

14. The method of manufacturing a ferroelectric memory device as defined in claim 13, further comprising a step of removing the surface-modifying film after forming the second electrode.

15. The method of manufacturing a ferroelectric memory device as defined in claim 13, wherein the surface-modifying film is formed on an entire surface of the first electrode and the ferroelectric film, and selectively removed in a region which becomes the first region to form the surface-modifying film only in the second region.

16. The method of manufacturing a ferroelectric memory device as defined in claim 2,

wherein a field effect transistor is provided with a gate electrode, a source region, and a drain region which are formed on the base, and wherein the ferroelectric memory device has a structure in which the first region corresponds to the electrode section connected to at least one of the source region and the drain region.

17. The method of manufacturing a ferroelectric memory device as defined in claim 7,

wherein a field effect transistor provided with a gate electrode, a source region, and a drain region which are formed on the base, and wherein the ferroelectric memory device has a structure in which the first region corresponds to the electrode section connected to at least one of the source region and the drain region.

18. The method of manufacturing a ferroelectric memory device as defined in claim 11,

wherein a field effect transistor provided with a gate electrode, a source region, and a drain region which are formed on the base, and wherein the ferroelectric memory device has a structure in which the first region corresponds to the electrode section connected to at least one of the source region and the drain region.

19. The method of manufacturing a ferroelectric memory device as defined in claim 1,

wherein a material for forming at least one member of the capacitor section is selectively deposited in the first region by providing a material for forming the at least one member of the capacitor section using vapor phase growth.

20. The method of manufacturing a ferroelectric memory device as defined in claim 19,

wherein the vapor phase growth is chemical vapor deposition and a selective deposition process is carried out in the first region.

21. The method of manufacturing a ferroelectric memory device as defined in claim 1,

wherein the second region is formed above the first region.

22. The method of manufacturing a ferroelectric memory device as defined in claim 21 which comprises two or more the first regions,

wherein a partition member is formed between the first regions, and wherein the second region is formed on the partition member.

23. The method of manufacturing a ferroelectric memory device as defined in claim 22,

wherein the partition member is formed on the base, and wherein the second region is formed at least on a surface of the partition member opposite to the base.

24. The method of manufacturing a ferroelectric memory device as defined in claim 22,

wherein the thickness of the partition member is equal to or greater than the thickness of the capacitor section.

25. The method of manufacturing a ferroelectric memory device as defined in claim 22, further comprising a step of removing the partition member.

26. A method of manufacturing a ferroelectric memory device provided with a capacitor section having a structure in which a base, a first electrode, a ferroelectric film, and a second electrode are deposited, the method comprising the steps of:

forming, on a surface of the base, a first region having surface characteristics allowing a material for forming at least one of the first electrode, the ferroelectric film, and the second electrode of the capacitor section to be preferentially de-

posited, and a second region having surface characteristics allowing a material for forming at least one member of the capacitor section to be less deposited than the first region, and formed above the first region; and
 5 providing a material for forming at least one member of the capacitor section to selectively form the member in the first region.

27. The method of manufacturing a ferroelectric mem- 10
 ory device as defined in claim 26,

wherein the surface of the base is exposed in the first region, and
 wherein a surface of the second region is a surface-modifying film of which affinity to the materials for forming the members of the capacitor section is lower than an affinity of the exposed surface in the first region.

28. The method of manufacturing a ferroelectric mem- 20
 ory device as defined in claim 27, further comprising a step of removing the surface-modifying film after forming at least one of the first electrode, the ferroelectric film, and the second electrode. 25

29. A ferroelectric memory device manufactured using a method as defined in any one of claims 1 to 25.

30. A ferroelectric memory device manufactured using 30
 a method as defined in any one of claims 26 to 28.

31. A ferroelectric memory device comprising:

a base having a first region and a second re- 35
 gion;
 a first electrode formed in the first region;
 a ferroelectric film formed on the first electrode;
 and
 a second electrode formed on the ferroelectric 40
 film,
 wherein the second region has surface characteristics allowing a material for forming at least one of the first electrode, the ferroelectric film, 45
 and the second electrode to be less deposited than a surface of the first region.

32. The ferroelectric memory device according to claim 31,
 wherein the second region is formed above a 50
 surface of the first region of the base.

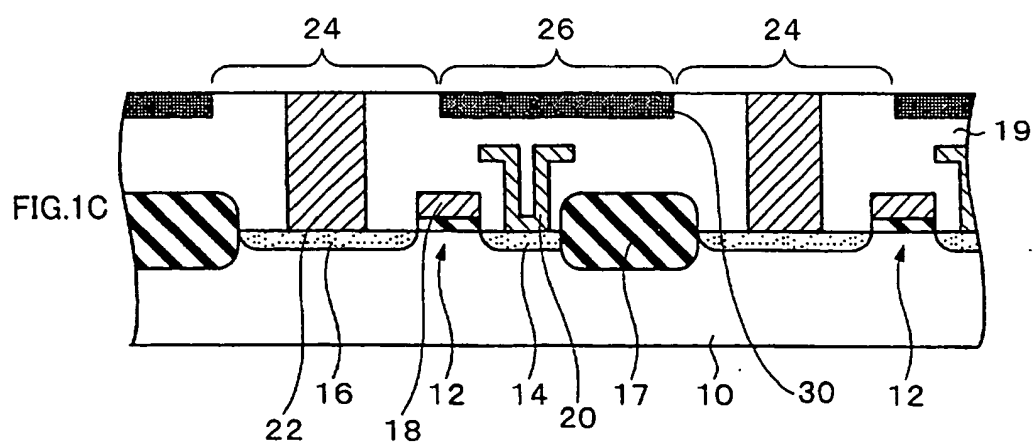
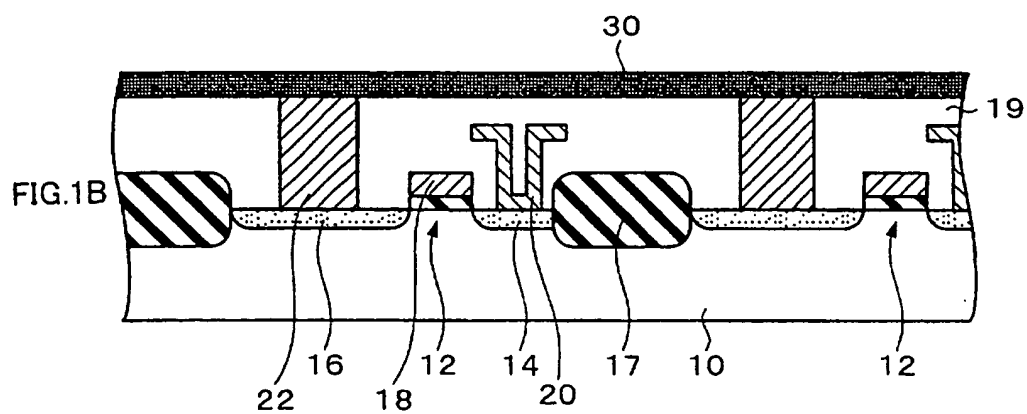
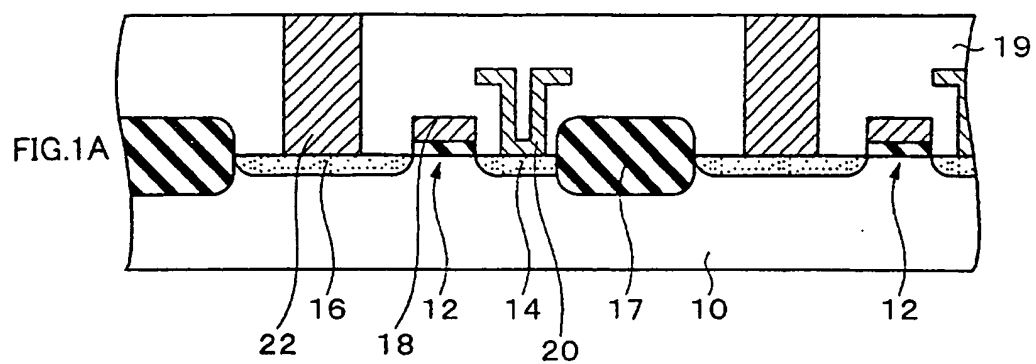
33. A ferroelectric memory device comprising:

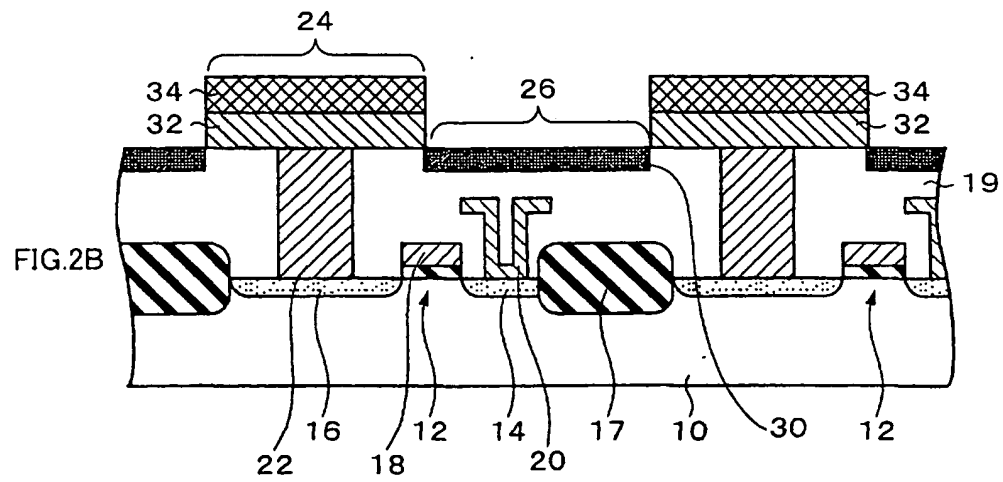
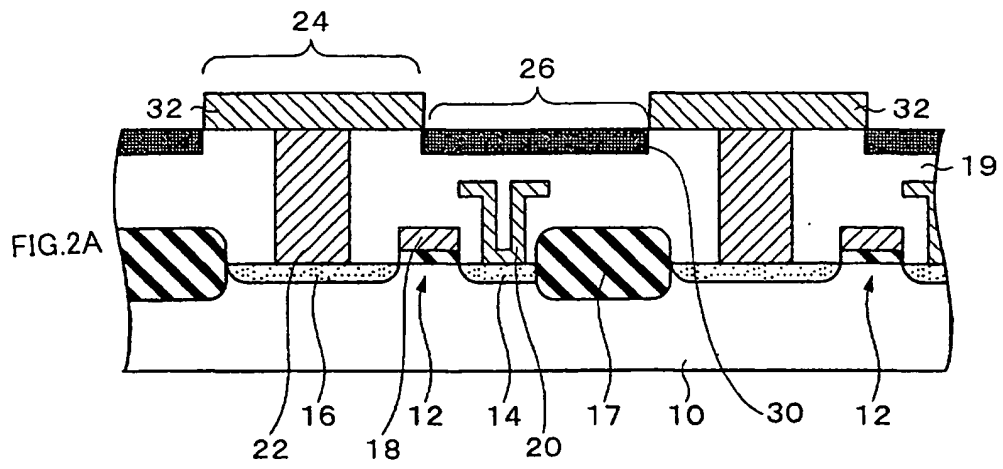
a first electrode formed on a base; 55
 a ferroelectric film formed on the first electrode;
 and
 a second electrode formed on the ferroelectric

film,
 wherein the base and the first electrode have surface characteristics allowing a material for forming the second electrode to be less deposited than a surface of the ferroelectric film on which the second electrode is formed.

34. The ferroelectric memory device as defined in claim 31,
 wherein a transistor connected to at least one of the first electrode and the second electrode is formed on the base.

35. The ferroelectric memory device as defined in claim 33,
 wherein a transistor connected to at least one of the first electrode and the second electrode is formed on the base.





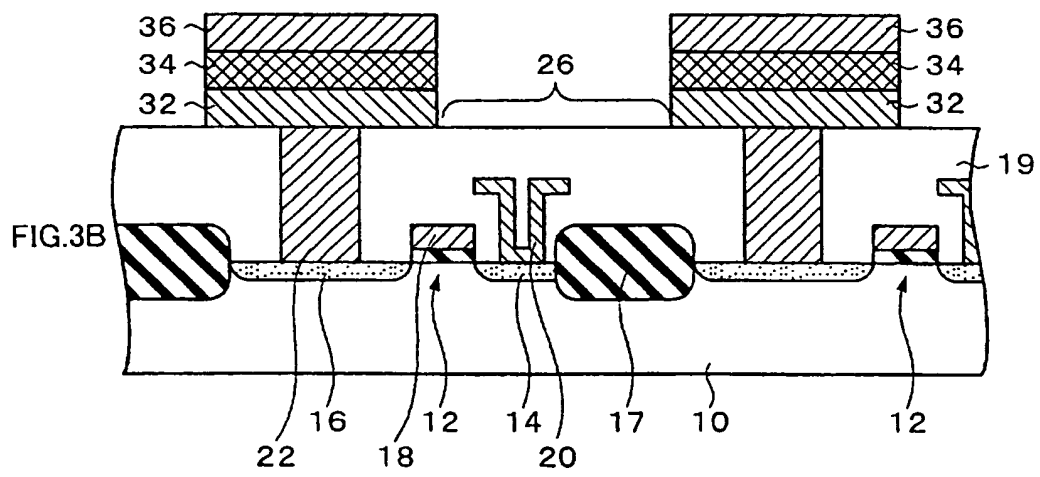
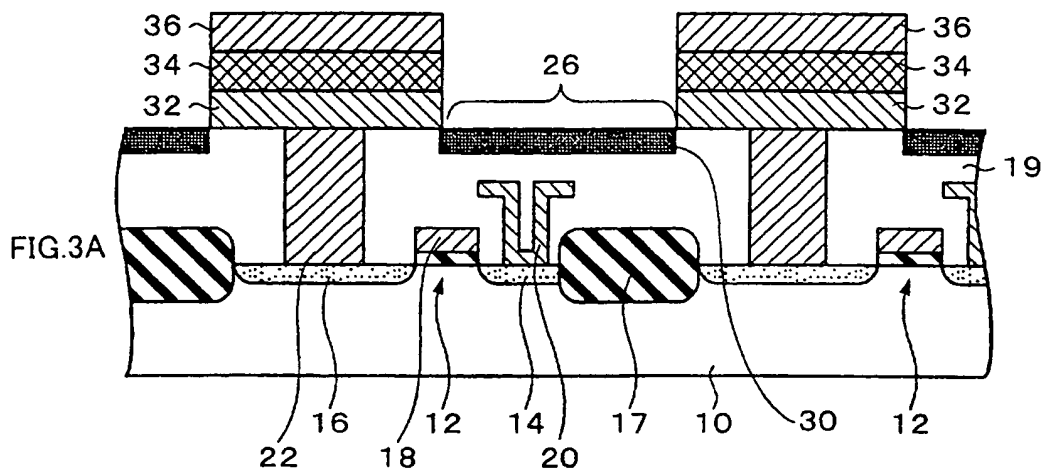


FIG.4

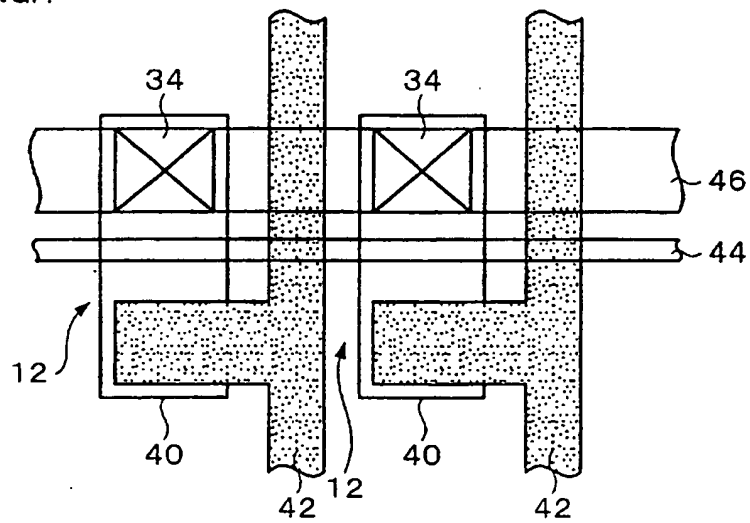
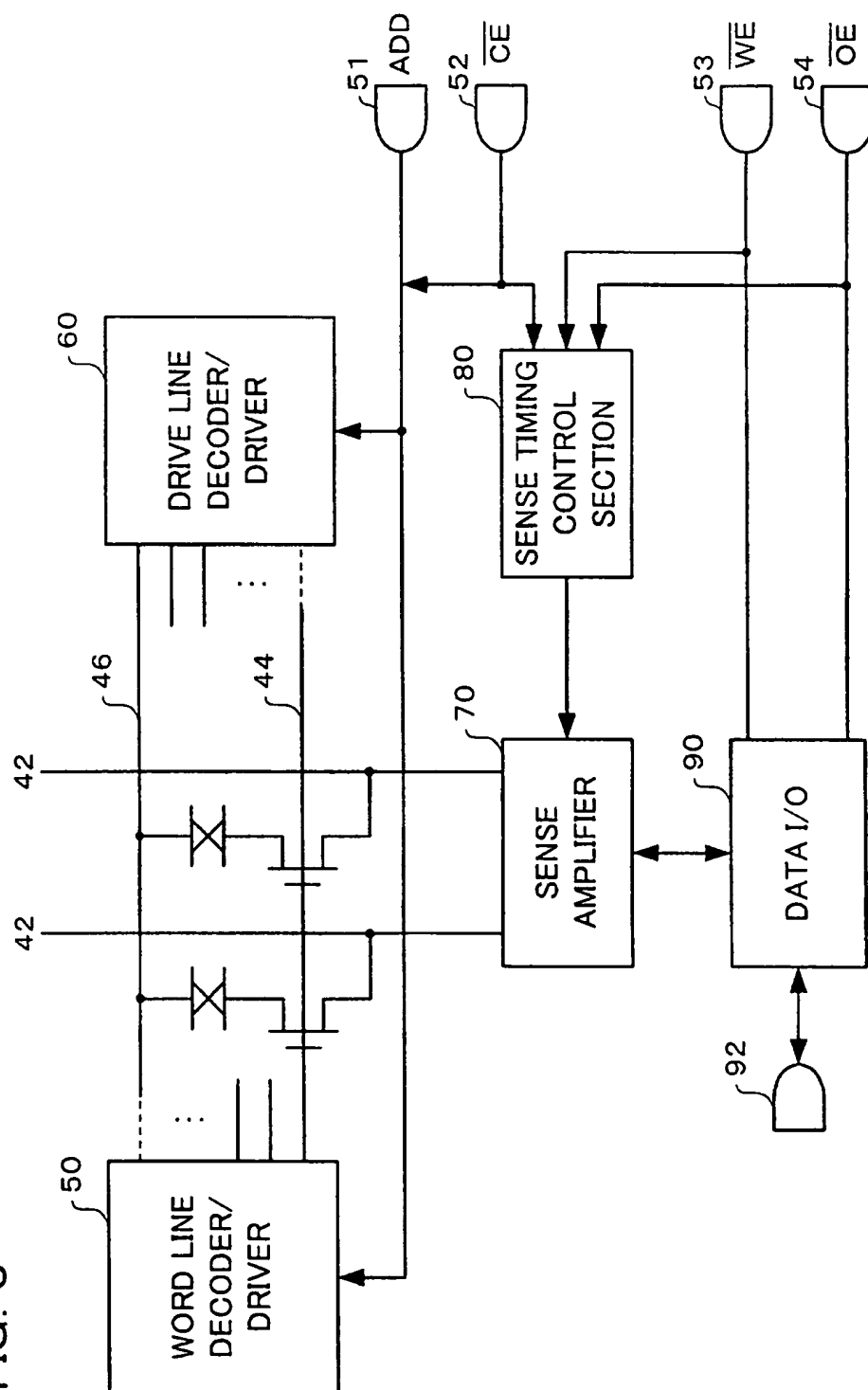
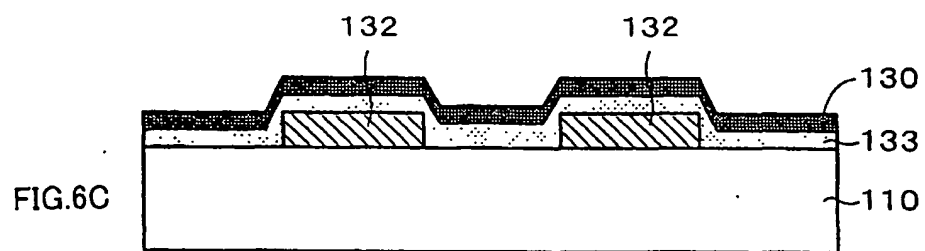
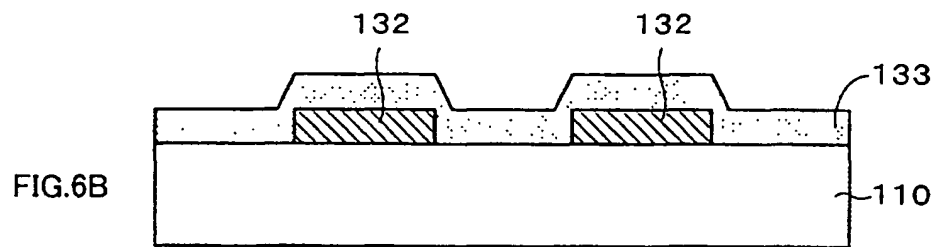
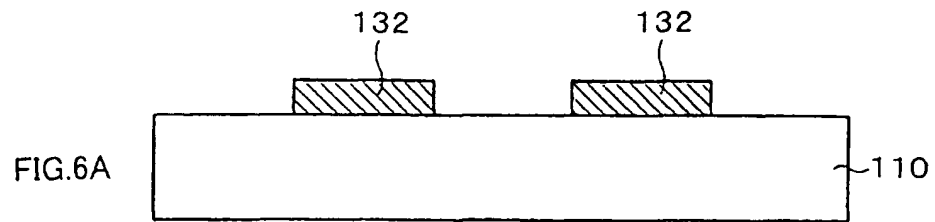
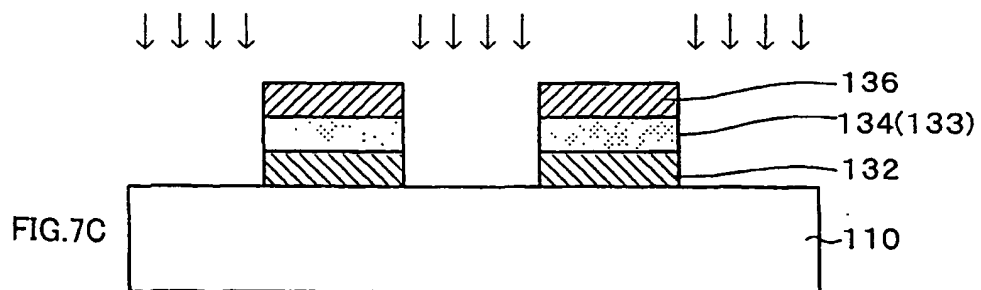
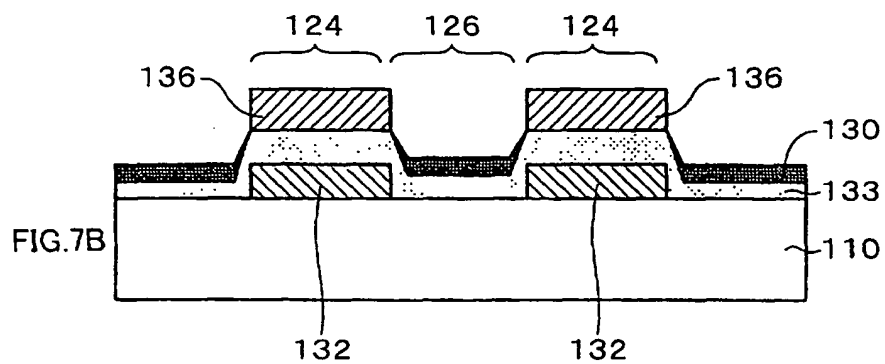
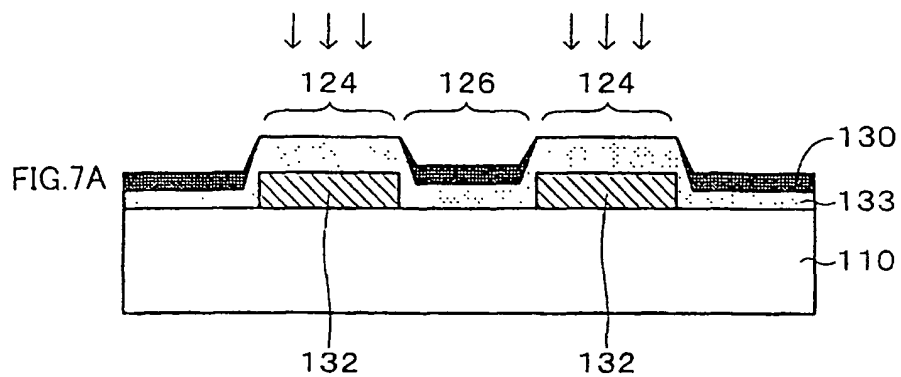
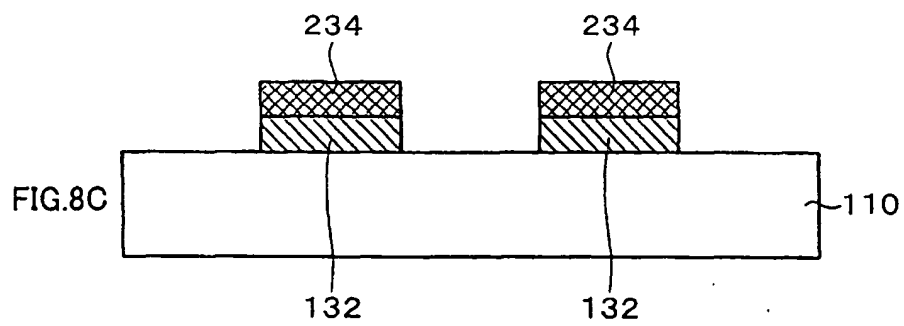
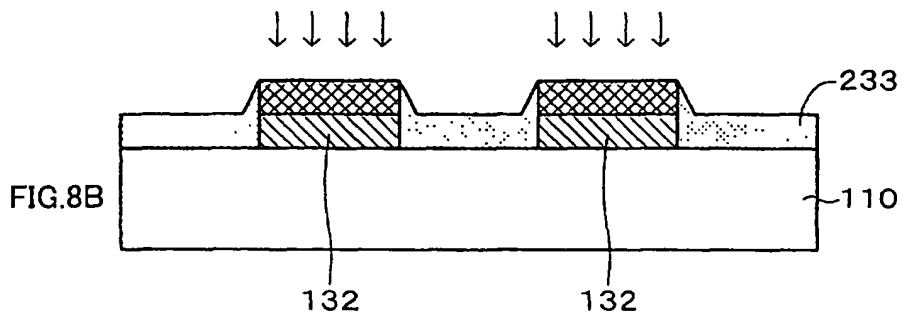
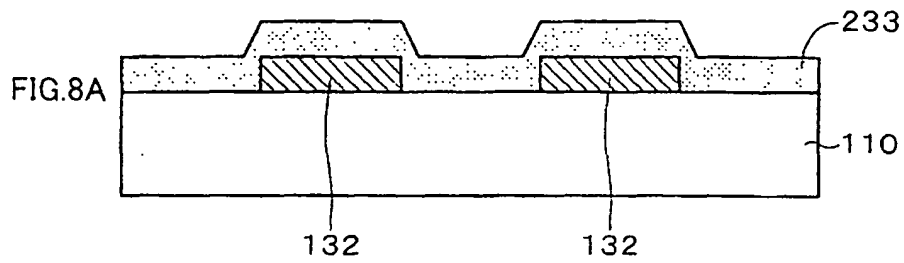


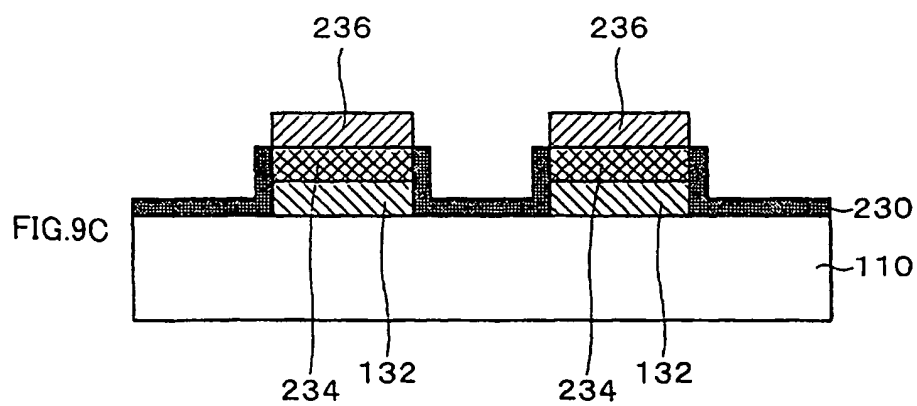
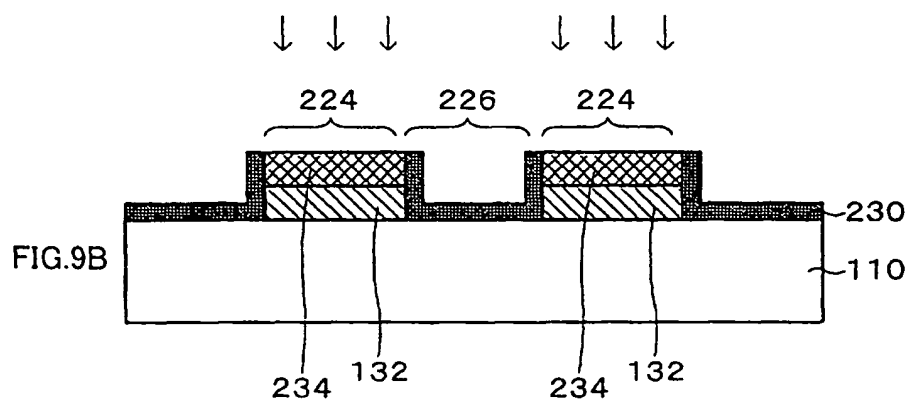
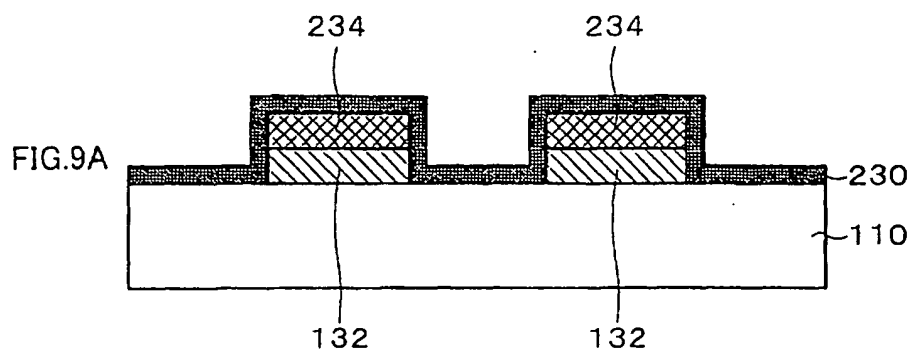
FIG. 5

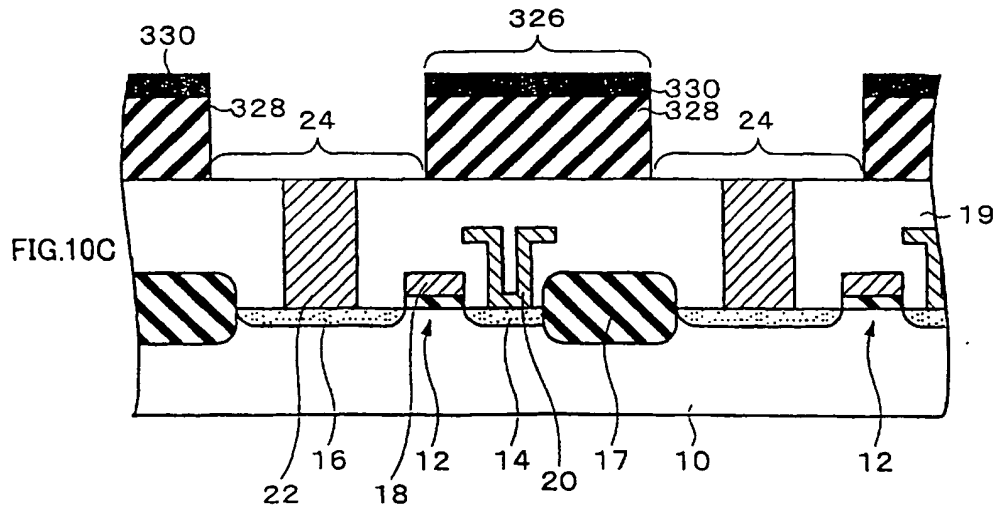
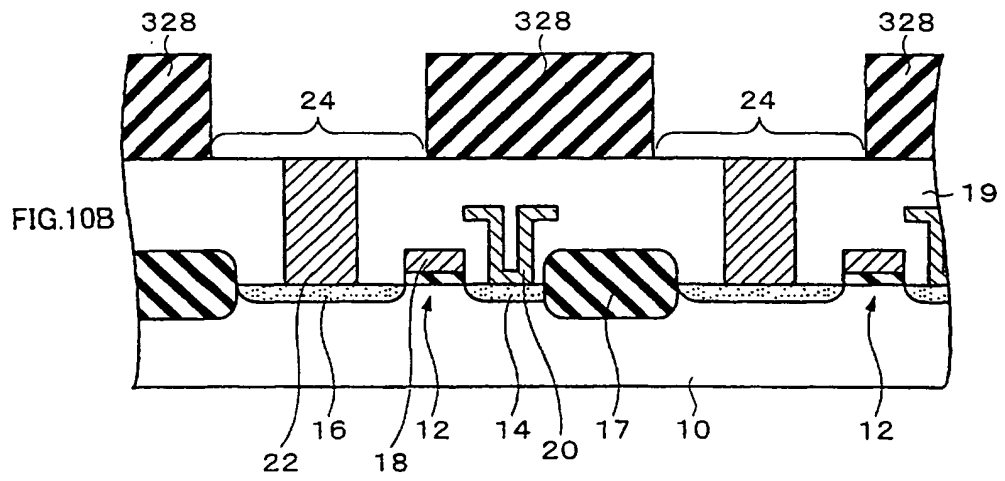
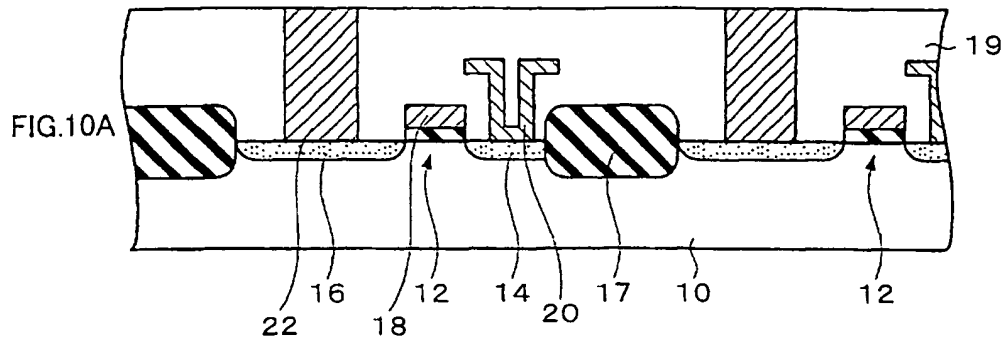


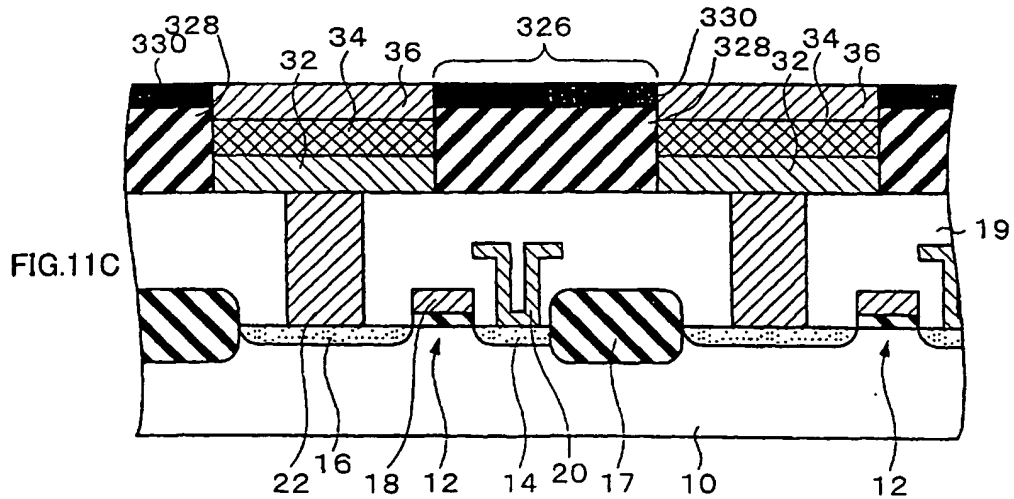
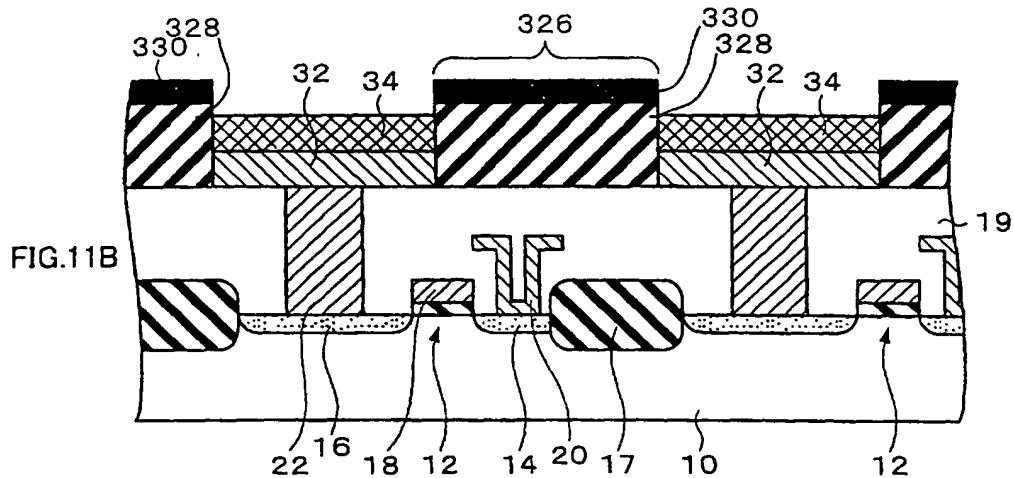
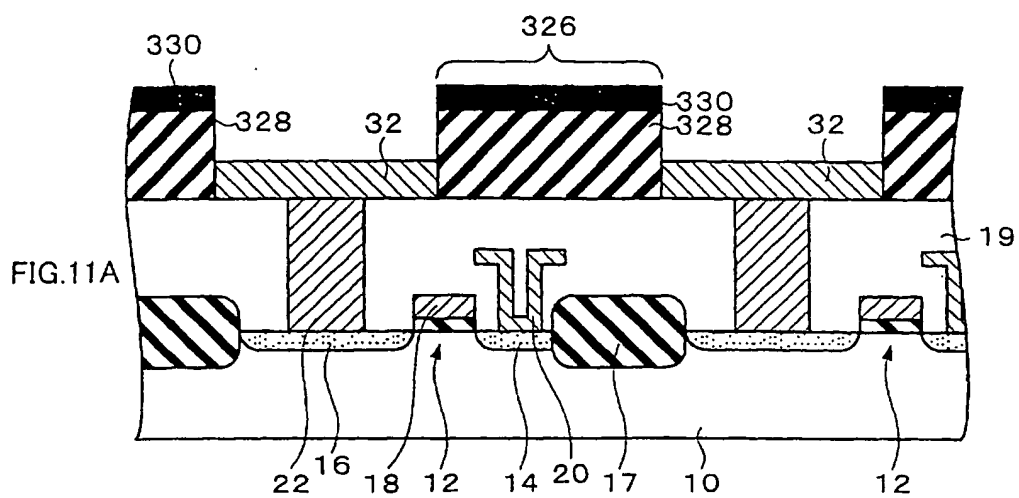


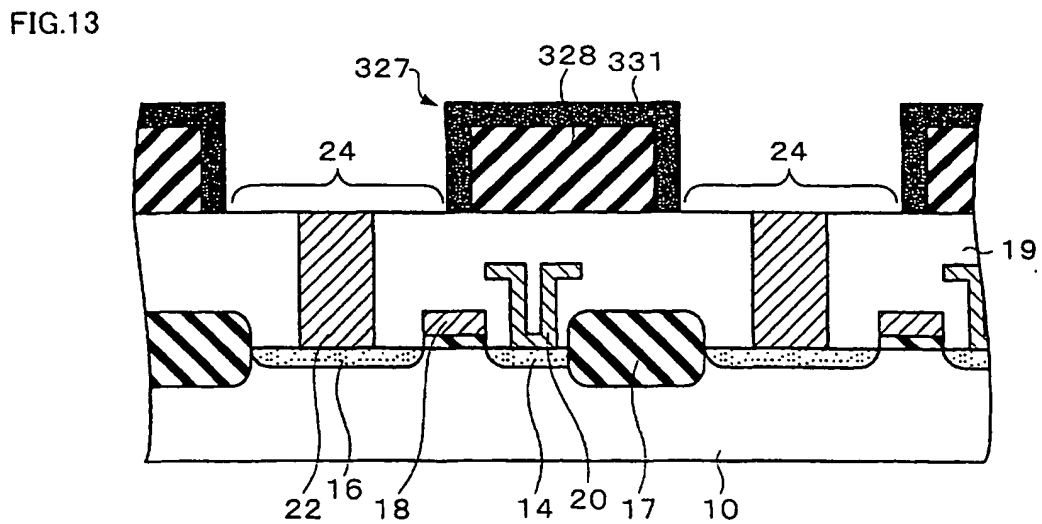
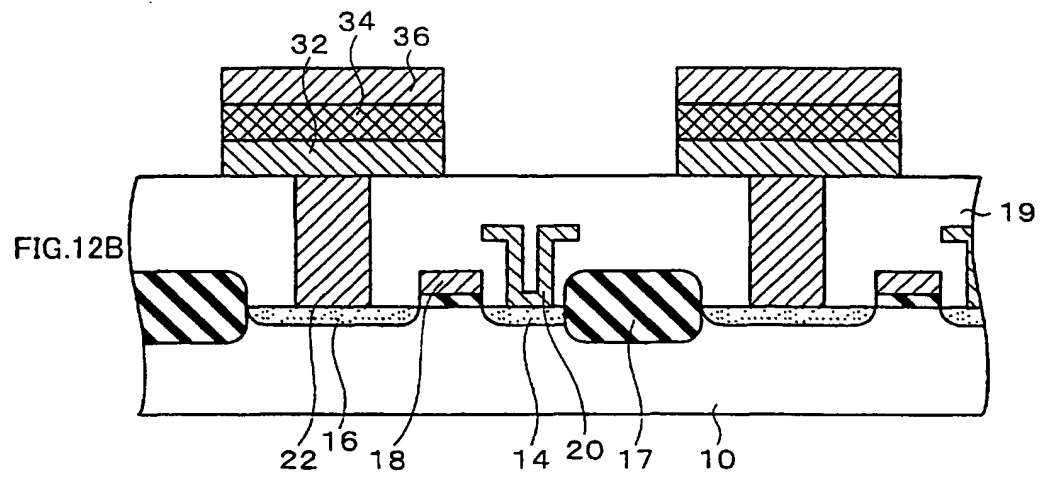
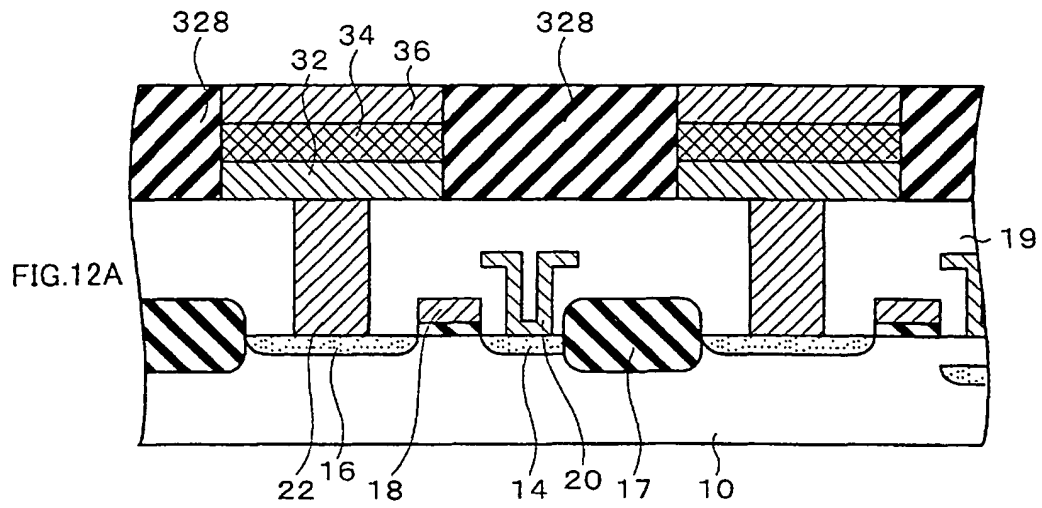












INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP00/03590

A. CLASSIFICATION OF SUBJECT MATTER Int.Cl. ⁷ H01L27/10, H01L27/108, H01L21/8242		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Int.Cl. ⁷ H01L27/10, H01L27/108, H01L21/8242 C23C16/50		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched. Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2000 Kokai Jitsuyo Shinan Koho 1971-2000 Jitsuyo Shinan Toroku Koho 1996-2000		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, 5874364, A (Fujitsu Limited), 23 February, 1999 (23.02.99), Column 33, line 32 to Column 34, line 16 & JP, 9-249972, A	1-4, 7, 8, 11, 16-20, 29, 31, 33-35
A	Claims 1 to 4; Column 10, line 4 to Column 11, line 20 & JP, 8-260148, A & JP, 9-82666, A & JP, 9-92795, A & JP, 9-246214, A	5, 6, 9, 10, 12-15, 21-28, 30
X	JP, 09-223778, A (Hitachi, Ltd.), 26 August, 1997 (26.08.97), Column 3, lines 6 to 50; Column 4, lines 18 to 46 (Family: none)	1-4, 7, 8, 11, 16-20, 29, 31, 33-35
A		5, 6, 9, 10, 12-15, 21-28, 30
X	US, 5686151, A (Kabushiki Kaisha Toshiba), 11 November, 1997 (11.11.97), Column 11, line 66 to Column 12, line 59 & JP, 7-86270, A	1-4, 7, 8, 11, 16-20, 29, 31, 33-35
A	Column 5, lines 2 to 46	5, 6, 9, 10,
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents; such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 24 August, 2000 (24.08.00)		Date of mailing of the international search report 05 September, 2000 (05.09.00)
Name and mailing address of the ISA/ Japanese Patent Office		Authorized officer
Facsimile No.		Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP00/03590

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	& JP, 7-273216, A & KR, 000139876, B	12-15, 21-28, 30
X	EP, 834912, A (TEXAS INSTRUMENTS INCORPORATED), 02 October, 1997 (02.10.97),	29-35
A	Column 14, lines 5 to 32 & JP, 10-107223, A See Figs. 19, 25, 47; relevant descriptions	1-28
X	JP, 10-50956, A (Hitachi, Ltd.), 20 February, 1998 (20.02.98), Column 6, lines 7 to 40 (Family: none)	29-35
X	JP, 11-8355, A (NEC Corporation), 12 January, 1999 (12.01.99), Column 5, line 25 to Column 6, line 18 (Family: none)	29-35
A	US, 5627013, A (Rohm Co., Ltd), 06 May, 1997 (06.05.97), Claims 1, 2 & JP, 5-136471, A Claim 1 & US, 5846686, A	12

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